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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/227,174
Filing Date: January 07, 1999
Appellant(s): PIAZZA ET AL.

Paul A. Mendonsa
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 24, 2003 appealing from the Office action mailed May 27, 2003.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is substantially correct. The appellants provide a statement that "Claim 35 stands rejected under 35U.S.C. 103(a) as being unpatentable over Eto, Fujinami, Hocevar, and further in view of U.S. Patent No. 5,446,495 issued to Tortier et al. (Tortier)". Tortier should be changed to "Tourtier", and therefore the status should be "Claim 35 stands rejected under 35U.S.C. 103(a) as being unpatentable over Eto, Fujinami, Hocevar, and further in view of U.S. Patent No. 5,446,495 issued to Tourtier et al. (Tourtier)"

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. "Tortier" as indicated in items 4 and 5 as shown in the Issues (Section VI) of the brief should be changed to "Tourtier", respectively. In addition, the rejection of claim 33 under 35 U.S.C. 112, second paragraph is another issue presented for appeal.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 29, 31, 32, 41, 42, 45 and 48 stand or fall together as Claim Group I; claims 33, 34, 43, 44, 46, 47, 49, and 50 stand or fall together as Claim Group II; claims 30 and 36-39 stand or fall together as Claim Group III; claim 35 stands or falls as Claim Group IV; and claim 40 stands or falls as Claim Group V.

(8) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) **Prior Art of Record**

5,652,823	ETO et al	7-1997
5,337,086	FUJINAMI	8-1994
6,002,438	HOCEVAR et al	12-1999
5,892,518	MIZOBATA et al	4-1999
6,208,350	HERRERA	3-2001
5,446,495	TOURTIER et al	8-1995

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claim 33 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 33, lines 2-4, the phrase "wherein a command stream controller to manipulate motion compensated video data comprises a command stream controller coupled to receive an instruction to manipulate motion compensated video" as claimed is vague and indefinite in that it seems to be claiming redundant limitations. In addition, it is unclear how a command stream controller comprises a command stream controller as claimed and it is unclear what the command stream controller is coupled to as claimed.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 29, 31, 32, 41, 42, 45, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eto et al of record (5,652,823) in view of Fujinami of record (5,337,086) and Hocevar et al (6,002,438).

Eto et al discloses a video data encoder and decoder as shown in Figures 1, 2, 7, and 15, and the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as claimed in claims 29, 31, 41, 42, 45, and 48 comprising substantially the same command stream controller (i.e., 17 of Figure 7 and see

column 24, lines 14-36) to manipulate motion compensated video data; a write address generator coupled to the command stream controller (see column 35, lines 13-30); a memory (i.e., 16 of Figure 7) coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator and based on an output from an Inverse Discrete Cosine Transform operation (see Figure 2, 12 of Figure 7, Figure 15I, column 4, column 24, lines 5-13, and column 35, lines 13-30); processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame (see Figures 2 and 7); a read address generator (see column 35, lines 13-30) coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output the pixel data in a second order (see Figure 15J, column 4, and column 35, lines 13-30); wherein the first order corresponds to an output sequence of an inverse discrete cosine transform operation (see Figure 2 and column 24, lines 5-13); receiving a motion compensation command (i.e., decoding control circuit 25 of Figure 7, see column 24, lines 5-67) having associated correction data related to a macroblock; storing the correction data in a memory (i.e., 16 of Figure 7 and see Figure 15I, column 4, column 35, lines 13-30) block by block according to a first order; performing frame prediction operations (see Figure 2) in response to the motion compensation command; reading the correction data from the memory (see Figure 15J, column 4, and column 35, lines 13-30); combining the correction data with results from the frame prediction operations to generate an output video frame (i.e., as provided by 413 of Figure 2, see column 4, column 24, lines 5-67);.

Eto et al does not particularly disclose, though, the followings:

(a) wherein the second order comprises reading the pixel data sub-block-by-sub-block row major order as claimed in claims 29 and 41; and

(b) wherein the first order is block by block in row major order, storing the correction data in a memory block by block in row major order, and reading the correction data from the memory sub-block by sub-block in row major order as claimed in claims 32, 42, 45, and 48.

Regarding (a) and (b), Fujinami discloses an image signal coding and decoding apparatus with multiple process motion compensation as shown in Figures 1, 3-6, and teaches the conventional breakdown of macroblocks into subblocks and the use of a read address generator for the selection of macroblock or subblock motion compensation processings (see column 4, lines 39-52, columns 7-9, Figures 1 and 6). It is noted that Fujinami is silent as to whether the blocks and subblocks stored and retrieve from memory are based on the row major orders as claimed. However, Hocevar et al discloses a method and apparatus for storing decoded video information as shown in Figures 1 and 2, and teaches the conventional storage and retrieval of blocks in a row major order fashion (see column 7, lines 9-48). It is hence considered obvious to provide the row major order storage and retrieval of blocks as taught by Hocevar et al as the specific method for the processing of data within the memory system of Fujinami. Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto et al, Fujinami, and Hocevar et al references in front of him/her and the general knowledge of block processings within motion compensation video systems, would have had no difficulty in providing a first order being block by block in row major order, storing the correction data in a memory block by block in row major order, reading the correction data from the memory sub-block by sub-block in row major order, and reading the pixel data in subblock by subblock major order as part of the

reading and writing of block and subblock data within Eto et al in view of the teachings of the combination of Fujinami and Hocevar et al for the same well known selective block processings as claimed.

4. Claims 33, 34, 43, 44, 46, 47, 49, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Eto, Fujinami, and Hocevar et al as applied to claims 29, 31, 32, 41, 42, 45, and 48 in the above paragraph (3), and further in view of Mizobata et al of record (5,892,518).

The combination of Eto, Fujinami, and Hocevar et al discloses substantially the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as above, but does not particularly disclose the followings:

(a) wherein performing frame prediction operations comprises generating a bounding box containing the macroblock, iterating the bounding box, fetching reference pixels, filtering the reference pixels, averaging the filtered reference pixels, if necessary, and adding correction data to the reference pixels as claimed in claims 46 and 49;

(b) performing texturing operations for the macroblock as claimed in claims 47 and 50; and

(c) the processing circuitry comprises a setup engine that determines a bounding box for pixels manipulated by the command, wherein the bounding box contains all edges of a macroblock and wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the bounding box are processed as claimed in claims 33, 34, 43 and 44.

Regarding (a) to (c), Mizobata et al discloses an image generating apparatus with pixel calculation circuit including texture mapping and motion compensation as shown in Figures 1, 2, 4A, 4B, 9, 10-12, 14A, 14B, 16, 17, 19A, 19B, 21, 22, 40, 41, and 43, and teaches substantially the same frame prediction operations comprising means for generating a bounding box, means for iterating the bounding box, means for fetching reference pixels, means for filtering the reference pixels, means for averaging the filtered reference pixels, if necessary, and means for adding correction data to the reference pixels (see 3009, 3010 of Figure 40, Figures 9-12, and 41-43); means for performing texturing operations for the macroblock (see Figures 10-12, and columns 28-30); and processing circuitry comprising a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock and wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the bounding box are processed (see Figures 9-12, 40-43). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, Hocevar et al, and Mizobata et al references in front of him/her and the general knowledge of motion compensation and texture image processings, would have had no difficulty in providing the bounding box of macroblock data including the manipulation of pixels thereby containing all edges of a macroblock as well as texture operations as taught by Mizobata et al for the video imaging system of Eto for the same well known purposes as claimed.

5. Claims 30 and 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Eto, Fujinami, and Hocevar et al as applied to claims 29, 31, 32, 41, 42, 45, and 48 in the above paragraph (3), and further in view of Herrera of record (6,208,350).

The combination of Eto, Fujinami, and Hocevar et al discloses substantially the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as above, further including a processing unit coupled to the read address generator and to the command stream controller, the processing unit to perform motion compensation operations (see Figures 2 and 7); memory to store reference pixels (see 407, 408 of Figure 2); mapping address generator to provide read addresses for the reference pixels (see column 35, lines 13-30); a first in first out buffer (see Figure 8); the read address generator coupled to a write address generator, the write address generator to generate synch points and the read address generator to receive the synch points to prevent the read address generator from overwriting valid data in the memory (see column 24, lines 46-62, column 35, lines 13-30).

The combination of Eto, Fujinami, and Hocevar et al does not particularly disclose, though, the processing unit/processing circuitry to perform texture mapping operations utilizing common circuitry; a bilinear filter coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels; the first in first out buffer coupling the mapping address generator to the bilinear filter, the buffer to maintain sequence of the read addresses from the mapping address generator to the bilinear filter as claimed in claims 30, 36, and 38. However, Herrera discloses a method and apparatus for processing DVD video as shown in Figures 1 and 7, and teaches the conventional texture mapping operations and

bilinear filterings within motion compensation systems (see column 14, lines 45-60). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, Hocevar et al, and Herrera references in front of him/her and the general knowledge of motion compensation video systems, would have had no difficulty in providing the texture mapping operations and bilinear filterings of Herrera within the motion compensated video system of Eto for further providing substantially the same if not the same texture mapping operations utilizing common circuitry, the bilinear filtering coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels, and the first in first out buffer coupling the mapping address generator to the bilinear filter purposes as claimed.

6. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Eto, Fujinami, and Hocevar et as applied to claims 29, 31, 32, 41, 42, 45, and 48 in the above paragraph (3), and further in view of Tourtier et al of record (5,446,495).

The combination of Eto, Fujinami, and Hocevar et al discloses substantially the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as above, but does not particularly disclose wherein the circuit is pipelined as claimed in claim 35. However, the particular motion compensation pipeline processings are old and well recognized in the art, as exemplified by Tourtier et al (see Figures 5 and 7). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, Hocevar et al, and Tourtier et al references in front of him/her and the general knowledge of pipeline processings within motion compensation video systems, would have had no difficulty in providing the multiple frame prediction operations in response to multiple motion

compensation commands in a pipeline manner as taught by Tourtier et al as part of the motion compensation video system of Eto for the same well known purposes as claimed.

7. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eto, Fujinami, Hocevar et al, and Herrera as applied to claims 29-32, 36-39, 41, 42, 45, and 48 in the above paragraphs (3) and (5), and further in view of Tourtier et al of record (5,446,495).

The combination of Eto, Fujinami, Hocevar et al, and Herrera discloses substantially the same method of motion compensation of digital video data, circuit for generating motion compensated video, and article of manufacture as above, but does not particularly disclose the apparatus is pipelined as claimed in claim 40. However, the particular motion compensation pipeline processings and multiple frame prediction operations are old and well recognized in the art, as exemplified by Tourtier et al (see Figures 5 and 7). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, Hocevar et al, Herrera, and Tourtier et al references in front of him/her and the general knowledge of pipeline processings within motion compensation video systems, would have had no difficulty in providing the multiple frame prediction operations in response to multiple motion compensation commands in a pipeline manner as taught by Tourtier et al as part of the motion compensation video system of Eto for the same well known purposes as claimed.

(11) Response to Argument

The appellants argued in the Brief filed November 24, 2003 concerning in general the rejection of claims 29, 31, 32, 41, 42, 45, and 48 in view of Eto, Fujinami, and Hocevar, and specifically that "...Whether these references teach the above cited limitations, they do not provide any suggestion or motivation that the references can be combined. In other words, the

simple assertion that Eto discloses reading and writing data in one order and that a combination of Fujinami and Hocevar discloses reading and writing data in another order does not reflect the complexity of reading data out in a different order from which it was originally written ... Identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention ...". The Examiner wants to point out again that Eto nevertheless teaches the particular read address generator (see column 35, lines 13-30) that causes the memory to output the pixel data in a second order (see Figure 15J, column 4, and column 35, lines 13-30). And since Fujinami teaches the conventional breakdown of macroblocks into subblocks with the use of a read address generator for the selection of macroblock or subblock motion compensation processings (see column 4, lines 39-52, columns 7-9, Figures 1 and 6 of Fujinami, and since Hocevar teaches the conventional storage and retrieval of blocks in a row major order (see column 7, lines 9-48 of Hocevar), it is hence considered obvious to provide the row major order storage and retrieval of blocks as taught by Hocevar as the specific method for processing of data within the memory system of Fujinami. The applicants' attention are directed to column 7, lines 20-24 of Hocevar et al with reference to Figure 2, wherein Hocevar et al teaches the particular retrieval (read out) of blocks 216, 218, 220, 228, 230, 232, 240, 242, and 244 in a row major order for motion compensation of a block of interest. In fact, Hocevar et al teaches a more beneficial system wherein block boundaries are added to the stored information and wherein the block boundaries are stored in a separate pointer table which points to the beginning of each block within the stored picture, thereby making it possible to locate the beginning of each block when it is necessary to retrieve a portion of the picture for motion compensation. Further, Hocevar et al at column 7, lines 49-65 teaches the

conventional row by row data (i.e., reading of the data in row major order) flow of displaying pictures from stored compressed data. And again, since Fujinami teaches the particular breakdown of macroblocks into subblocks within storage device 1 and the use of a read address generator for the selection of macroblock or subblock motion compensation processings (see column 4, lines 39-52, columns 7-9, Figures 1 and 6), Fujinami thereby provides the particular reading pixel data out in a second order (i.e., subblock) that is different from the order (macroblock) in which the data was stored in memory (i.e., the stored macroblocks within frame memory 1 are provided/read out in the subblock format, see column 4, lines 39-52, column 7, lines 36-58). In addition, it is considered obvious again that the particular subblock data of Fujinami may certainly be provided within Hocevar et al for storage and read out in a row major order, and thereby rendering obvious the claimed invention. It is therefore submitted again that it is considered obvious to provide the first order being block by block in row major order, storing the correction data in a memory block by block in row major order, reading the correction data from the memory sub-block by sub-block in row major order, and reading the pixel data in subblock by subblock major order as part of the reading and writing of block and subblock of data within Eto et al in view of the teachings of the combination of Fujinami and Hocevar.

The appellants argued in the Brief filed November 24, 2003 concerning in general that "... Eto discusses a write/read control signal that triggers the temporal storage into memory of the output from a motion decoder. However, Eto fails to disclose a write address generator that determines the order in which pixel data will be written to memory and a read address generator that determines the order in which the data will be read out from memory as claimed by

Appellant ...". The Examiner respectfully disagrees. Such statements made by the appellants are somewhat contradictory. On the one hand, appellants state that Eto has a write/read control signal that triggers the temporal storage into memory, and on the other hand the appellants contend that Eto fails to disclose a write address generator and a read address generator. Memory 16 of Eto must inherently have write and read address generators since write/read control signals are used to control the data to and from the memory 16 (see column 35, lines 13-30). The Examiner wants to point out that: One of ordinary skill in the art is presumed to possess a certain amount of background knowledge independent of the references. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985); In re Jacoby, 309 F.2d 513, 135 USPQ 317 (C.C.P.A. 1962). The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (C.C.P.A. 1969).

The appellants argued in the Brief filed November 24, 2003 concerning the rejection of claims 33, 34, 43, 44, 46, 47, 49, and 50 in view of the combination of Eto, Fujinami, Hocevar, and Mizobata, and specifically that "... Whether Mizobata discloses the limitations cited by the Final Office Action, it does not teach or suggest storing pixel data in a first order and outputting pixel data in a second order as claimed by Appellant ...". The Examiner respectfully disagrees. The appellants' attention are directed to column 35, lines 13-30 and Figures 15I and 15J of Eto wherein it is taught that pixel data are stored in a first order (Figure 15I) and the pixel data are outputted in a second order (Figure 15J).

The appellants argued in the Brief filed November 24, 2003 concerning in general the rejection of claims 30 and 36-39 in view of the combination of Eto, Fujinami, Hocevar, and

Herrera, and specifically that "...Whether or not Herrera discloses the limitations cited by the Final Office Action, it does not teach or suggest storing pixel data in a first order and outputting pixel data in a second order as claimed by Appellant ... Herrera, in contrast, discloses a combination of a modified graphics accelerator with software to create a cost effective hybrid solution to providing a personal computer with DVD capabilities ... Herrera, therefore, explicitly teaches away from Eto, rather than providing an implicit basis to combine the references ...". The Examiner wants to point out again that Eto (see column 35, lines 13-30) nevertheless teaches pixel data being stored in a first order (Figure 15I) and the pixel data are outputted in a second order (Figure 15J). Though Herrera may teach a modified graphics accelerator and various features different from the claimed invention, the critical issue at hand is that it is nevertheless that Herrera (see column 14, lines 45-60) teaches the particular texture mapping operations and bilinear filterings associated with motion compensation systems that may obviously be performed within the motion compensation video system of Eto so as to carry out substantially the same if not the same texture mapping operations utilizing common circuitry, the bilinear filtering coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels, and the first in first out buffer coupling the mapping address generator to the bilinear filter purposes as claimed.

The appellants argued in the Brief filed November 24, 2003 concerning the rejection of claim 35 in view of the combination of Eto, Fujinami, Hocevar, and Tourtier, and specifically that "... Whether or not Tourtier discloses the limitations cited by the Final Office Action, it does not teach or suggest storing pixel data in a first order and outputting pixel data in a second order as claimed by Appellant ... the simple reference to Tourtier, declaring that pipelining is

well-known generally, does not relieve the burden of demonstrating obviousness by a shown of particular findings of fact ... citing Tourtier does not, in and of itself, address the complexities of storing data in a first order and reading out data in a second order within the framework of pipelined circuitry ...". The Examiner wants to point out again that Eto (see column 35, lines 13-30) nevertheless teaches pixel data being stored in a first order (Figure 15I) and the pixel data are outputted in a second order (Figure 15J). It is submitted that the particular motion compensation pipeline processings as shown in Figures 5 and 7 of Tourtier may obviously be provided within the motion compensation video system of Eto, thereby rendering obvious the claimed invention.

The appellants argued in the Brief filed November 24, 2003 concerning in general the rejection of claim 40 in view of the combination of Eto, Fujinami, Hocevar, Herrera, and Tourtier, and specifically that "... Whether or not Tourtier discloses the limitations cited by the Final Office Action, it does not teach or suggest storing pixel data in a first order and outputting pixel data in a second order as claimed by Appellant ...". The Examiner wants to point out that such arguments have been addressed in the above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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August 17, 2006

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